REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The non-final Office Action dated December 29, 2003 has been received and its contents carefully reviewed.

By this Response, claims 1 and 10 have been amended, and claim 2 has been cancelled without prejudice or disclaimer of the subject matter recited therein. No new matter has been added. Applicant respectfully requests reconsideration of the present application in view of the above amendments and the following remarks. Claims 1 and 3-16 are pending.

In the Office Action, claims 1, 2 and 6-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,335,770, issued to Komatsu. Applicant traverses the rejection because Komatsu fails to teach or suggest each of the features recited in the claims of the present application. For example, Komatsu fails to teach or suggest an in-plane switching mode liquid crystal display device that includes, among other features:

> "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in independent claim 1;
>
> "a plurality of common voltage lines parallel to the gate lines and crossing the gate links, wherein the plurality of common voltage lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in independent claim 6; and
>
> "a plurality of common lines extending to cross the plurality of the gate links between the signal pads and the thin film transistor array, wherein the plurality of common lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the signal pad area", as recited in independent claim 10.

In order to anticipate, each of the recited elements must be taught by the applied reference. Komatsu teaches a single common voltage line. In particular, common bus line 103 is grounded through common pad" (col. 5, lines 39-47). Accordingly, Applicant respectfully

submits Komatsu fails to teach at least the above features and structure of independent claims 1, 6 and 10. Because Komatsu does not teach each element of the recited claims of the present application, rejected independent claim 1, rejected independent claim 6 and its dependent claims 7-10, and rejected independent claim 10 and its dependent claims 11-16 are not anticipated by Komatsu. Reconsideration and withdrawal of the rejection are requested.

In the Office Action, claims 1-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,456, 350, issued to Ashizawa et al. (hereafter "Ashizawa"). Applicant traverses the rejection because Ashizawa fails to teach or suggest each of the features recited in the claims of the present application. For example, Ashizawa fails to teach or suggest an in-plane switching mode liquid crystal display device having: an in-plane switching mode liquid crystal display device that includes, among other features:

> "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in independent claim 1;
>
> "a plurality of common voltage lines parallel to the gate lines and crossing the gate links, wherein the plurality of common voltage lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in independent claim 6; and
>
> "a plurality of common lines extending to cross the plurality of the gate links between the signal pads and the thin film transistor array, wherein the plurality of common lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the signal pad area", as recited in independent claim 10.

Applicant submits Ashizawa discloses in embodiment 3, FIG. 6, "the plurality of common bus lines CC1, CC2, CC3 are supplied to all of the common electrodes CT via the common voltage signal lines CL with relatively short routes" (col. 8, lines 41-44). As such, Ashizawa fails to teach a plurality of common voltage lines having the features recited independent claims 1, 6 and 10 of the present application. Because Ashizawa does not teach each element of the recited claims of the present application, rejected independent claim 1,

rejected independent claim 6 and its dependent claims 7-10, and rejected independent claim 10 and its dependent claims 11-16 are not anticipated by Ashizawa. Reconsideration and withdrawal of the rejection are requested.

In the Office Action, dependent claims 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ashizawa. Applicant traverses the rejection because Ashizawa, analyzed alone, fails to teach or suggest the combined features recited in the claims of the present application. For example, Ashizawa, as discussed above, fails to teach or suggest "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate voltage at the plurality of gate links, wherein the plurality of common voltage lines are arranged parallel to the plurality of gate lines", as recited in independent claim 1, from which rejected claims 3-5 depend.

By virtue of their dependence from independent claim 1, claims 3-5 also contain the allowable subject matter of claim 1. Because Ashizawa fails to teach or suggest at least the features of independent claim 1, claim 1 and its rejected dependent claims 3-5 are allowable over Ashizawa. Reconsideration and withdrawal of the rejection are requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500. If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: March 29, 2003

Respectfully submitted,

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